AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A magnetic random access memory comprising:

a plurality of bit lines extending in a first direction;

a reference bit line extending in the first direction;

a plurality of memory cells provided along said plurality of bit lines;

a plurality of reference cells provided along said plurality of reference bit lines; and

a read section,

wherein each of said plurality of memory cells has a first tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take a first state or a second state, and is connected to one of said plurality of bit lines in a read operation,

each of said plurality of reference cells has a reference tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take the first state or the second state and is

connected to one of said plurality of reference bit lines in the read operation,

said read section comprises:

a first resistance section having a first resistance value and having a ninth terminal serving as one terminal connected to a selected bit line and a tenth terminal serving as the other terminal connected to a first power supply in the read operation;

a second resistance section having a second resistance value different from the first resistance value and having an eleventh terminal serving as one terminal connected to said reference bit line and a twelfth terminal serving as the other terminal connected to the first power supply in the read operation; and

a comparing section configured to compare a sense voltage serving as a voltage of the ninth terminal with a reference voltage serving as a voltage of the eleventh terminal,

wherein when the data stored in a selected cell is read out, said read section generates said sense voltage by dividing the voltage of the first power supply by said first tunneling magnetic resistance and said first resistance section of the selected cell, and said reference voltage by dividing the voltage of the first power supply by said reference tunneling magnetic resistance and said second resistance section of a selected

reference cell, and outputs a comparison result between said sense voltage and said reference voltage, and

said selected cell is selected from said plurality of memory cells and said selected reference cell is selected from said plurality of reference cells.

2. (canceled)

3. (currently amended) ~~The magnetic random access memory according to claim 1,~~ A magnetic random access memory comprising:

a plurality of bit lines extending in a first direction;

a reference bit line extending in the first direction;

a plurality of memory cells provided along said plurality of bit lines;

a plurality of reference cells provided along said plurality of reference bit lines; and

a read section,

wherein each of said plurality of memory cells has a first tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take a first state or a second state, and is connected to one of said plurality of bit lines in a read operation,

each of said plurality of reference cells has a reference tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take the first state or the second state and is connected to one of said plurality of reference bit lines in the read operation,

said read section comprises:

a first resistance section having a first resistance value and having a ninth terminal serving as one terminal connected to a selected bit line and a tenth terminal serving as the other terminal connected to a first power supply in the read operation;

a second resistance section having a second resistance value different from the first resistance value and having an eleventh terminal serving as one terminal connected to said reference bit line and a twelfth terminal serving as the other terminal connected to the first power supply in the read operation; and

a comparing section configured to compare a sense voltage serving as a voltage of the ninth terminal with a reference voltage serving as a voltage of the eleventh terminal,

wherein said first resistance section has a spontaneous magnetization whose direction is reversed to take the first state or the second state and has a second tunneling magnetic

resistance and a third tunneling magnetic resistance connected in series, and

said second resistance section has a spontaneous magnetization whose direction is reversed to take the first state or the second state and has a fourth tunneling magnetic resistance and a fifth tunneling magnetic resistance connected in series.

4. (original) The magnetic random access memory according to claim 3, wherein said reference tunneling magnetic resistance, said first tunneling magnetic resistance, said second tunneling magnetic resistance, said third tunneling magnetic resistance, said fourth tunneling magnetic resistance, and said fifth tunneling magnetic resistance substantially have a same structure,

said second tunneling magnetic resistance and said third tunneling magnetic resistance are same in the magnetization direction of the spontaneous magnetization, and

said fourth tunneling magnetic resistance and said fifth tunneling magnetic resistance are different in the magnetization direction of the spontaneous magnetization.

5. (currently amended) ~~The magnetic random access memory according to claim 1, further comprising:~~

<u>A magnetic random access memory comprising:</u>

a plurality of bit lines extending in a first direction;

a reference bit line extending in the first direction;

a plurality of memory cells provided along said plurality of bit lines;

a plurality of reference cells provided along said plurality of reference bit lines; and

a read section,

wherein each of said plurality of memory cells has a first tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take a first state or a second state, and is connected to one of said plurality of bit lines in a read operation,

each of said plurality of reference cells has a reference tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take the first state or the second state and is connected to one of said plurality of reference bit lines in the read operation,

said read section comprises:

a first resistance section having a first resistance value and having a ninth terminal serving as one terminal connected to a selected bit line and a tenth terminal serving as

the other terminal connected to a first power supply in the read operation;

a second resistance section having a second resistance value different from the first resistance value and having an eleventh terminal serving as one terminal connected to said reference bit line and a twelfth terminal serving as the other terminal connected to the first power supply in the read operation;

a comparing section configured to compare a sense voltage serving as a voltage of the ninth terminal with a reference voltage serving as a voltage of the eleventh terminal; and

a breakdown voltage preventing circuit connected between said ninth terminal and said plurality of memory cells to prevent a voltage higher than a predetermined voltage from being applied to said plurality of memory cells.

6. (currently amended) ~~The magnetic random access memory according to claim 1,~~

A magnetic random access memory comprising:

a plurality of bit lines extending in a first direction;

a reference bit line extending in the first direction;

a plurality of memory cells provided along said plurality of bit lines;

a plurality of reference cells provided along said plurality of reference bit lines; and

a read section,

wherein each of said plurality of memory cells has a first tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take a first state or a second state, and is connected to one of said plurality of bit lines in a read operation,

each of said plurality of reference cells has a reference tunneling magnetic resistance which has spontaneous magnetization whose direction is reversed in accordance with data to be stored to take the first state or the second state and is connected to one of said plurality of reference bit lines in the read operation,

said read section comprises:

a first resistance section having a first resistance value and having a ninth terminal serving as one terminal connected to a selected bit line and a tenth terminal serving as the other terminal connected to a first power supply in the read operation;

a second resistance section having a second resistance value different from the first resistance value and having an eleventh terminal serving as one terminal connected to said reference bit line and a twelfth terminal serving as the other

terminal connected to the first power supply in the read operation; and

a comparing section configured to compare a sense voltage serving as a voltage of the ninth terminal with a reference voltage serving as a voltage of the eleventh terminal,

wherein said read section comprises:

a first constant voltage section configured to apply a second voltage between the ninth terminal and said plurality of memory cells and between the eleventh terminal and said plurality of reference cells;

a first current section provided between said first constant voltage section and the ninth terminal to supply said selected bit line and said first resistance section with a current having a same magnitude; and

a second current section provided between said first constant voltage section and the eleventh terminal to supply said reference bit line and said second resistance section with a current having a same magnitude.

7. (original) The magnetic random access memory according to claim 6, wherein when the data stored in the selected cell is read out,

said first constant voltage section applies a second voltage to said selected bit line and reference bit line,

said first current section supplies sense currents having a same magnitude to said selected bit line, selected cell, and first resistance section,

said second current portion supplies reference currents having a same magnitude to said reference bit line, said selected reference cell, and said second resistance section,

said read section compares said sense voltage as a voltage between said first current section and said second resistance section with said reference voltage as a voltage between said second current section and said second resistance section and outputs a comparing result, and

said selected bit line is selected from said plurality of bit lines, said selected cell is selected from said plurality of memory cells, and said selected reference cell is selected from said plurality of reference cells.

8. (original) The magnetic random access memory according to claim 6, wherein said first constant voltage section includes a clamp circuit.

9. (original) The magnetic random access memory according to claim 6, wherein at least one of said first current portion and said second current portion includes a current mirror circuit.

10. (original) The magnetic random access memory according to claim 6, wherein said read section further comprises at least one of a first auxiliary section and a second auxiliary section,

said first auxiliary section is connected to the ninth terminal and changeable said sense voltage, and

said second auxiliary section is connected to the eleventh terminal and changeable said reference voltage.

11. (original) The magnetic random access memory according to claim 10, wherein at least one of said first auxiliary section and said second auxiliary section includes a trimming circuit.

12. (original) The magnetic random access memory according to claim 1, wherein said plurality of reference cells further include first switches respectively connected to said reference tunneling magnetic resistances in series, and said reference cells are connected in parallel with said reference bit line, and

one of said plurality of reference cells is selected by one of said first switches as a selected reference cell used in the read operation.

13. (original) The magnetic random access memory according to claim 1, wherein there are a plurality of first resistance sections,

each of said plurality of first resistance sections is connected to the ninth and tenth terminals and has a second switch on either side of the ninth-terminal and the tenth-terminal, and

one of said plurality of first resistance sections is selected by one of said second switches as said first resistance section used in the read operation.

14. (original) The magnetic random access memory according to claim 1, wherein there are a plurality of second resistance sections,

each of said plurality of second resistance sections is connected to the eleventh and twelfth terminals and has a third switch on either side of the eleventh-terminal and twelfth-terminal, and

one of said plurality of second resistance sections is selected by one of said third switches as said second resistance section used in the read operation.

15. (original) The magnetic random access memory according to claim 1, wherein said reference voltage Vref is obtained from the following equation (1):

$$Vref = Vs(1)+k\cdot(Vs(2)+Vs(1)) \qquad (1)$$

where said sense voltage in the first state is Vs(1), and said sense voltage in the second state is Vs(2) in the following equation (1), and a variable k is equal to or less than 0.49.

16. (original) The magnetic random access memory according to claim 1, further comprising:

a plurality of word line pairs, each of which includes a first word line and a second word line extending in a second direction substantially perpendicular to the first direction;

a first selector configured to select a selected bit line from said plurality of bit lines and a reference bit line in the read operation;

a second selector configured to select a selected bit line from said plurality of bit lines in a write operation;

a third selector configured to select a selected first word line from said plurality of first word lines in the write operation; and

a fourth selector configured to select a second word line from said plurality of second word lines in the read operation,

wherein each of said plurality of memory cells further comprises:

a first transistor having a first gate connected to one of said plurality of second word lines, a first terminal serving as one of terminals other than the first gate, and a second terminal serving as the other terminal connected to ground,

each of said plurality of memory cells is provided to one of positions where said plurality of bit lines and said plurality of word line pairs are intersected,

said first tunneling magnetic resistance has a third terminal serving as one terminal connected to the first terminal and a fourth terminal serving as the other terminal connected to one of said plurality of bit lines,

each of said plurality of reference cells further comprises a second transistor having a second gate connected to the second word line, a fifth terminal serving as one of terminals other than the second gate and a sixth terminal serving as the other terminal connected to ground,

each of said plurality of reference cells is provided to one of positions where said plurality of reference bit lines and said plurality of word line pairs are intersected, and

said reference tunneling magnetic resistance has a seventh terminal serving as one terminal connected to the fifth terminal and an eighth terminal serving as the other terminal connected to the reference bit line.

17. (original) The magnetic random access memory according to claim 16, wherein when the data stored in a selected cell is read out,

said fourth selector first supplies a voltage to a selected second word line to turn on said first transistor of said selected cell and a voltage to unselected second word lines other than said selected second word line to turn off said first transistors of unselected cells,

said first selector connects said selected bit line and said reference bit line to said read section,

said read section divides the voltage of the first power supply by said first tunneling magnetic resistance and said first resistance section of said selected cell to generate said sense voltage, divides the voltage of the first power supply by said reference tunneling magnetic resistance of said selected reference cell and said second resistance section to generate said reference voltage, and outputs a comparing result of said sense voltage with said reference voltage, and

said selected cell is selected from said plurality of memory cells by said selected second word line and said selected bit line, said unselected cells are memory cells other than said selected cell, said selected reference cell is selected from said plurality of reference cells by said selected second word line and said reference bit line.

18. (original) The magnetic random access memory according to claim 1, further comprises:

a word line extending in the second direction substantially perpendicular to the first direction;

a first selector configured to select said selected bit line from said plurality of bit lines and to select a reference bit line in the read operation; and

a second selector configured to select a selected word line from said plurality of word lines,

wherein each of said plurality of memory cells is provided to one of positions where said plurality of bit lines and said plurality of word lines are intersected,

said first tunneling magnetic resistance has a first terminal serving as one terminal connected to said word line and a second terminal serving as the other terminal connected to the bit line,

each of said plurality of reference cells is provided to one of positions where said reference bit line and said plurality of word lines are intersected, and

said reference tunneling magnetic resistance has the third terminal serving as one terminal connected to said word line and the fourth terminal serving as the other terminal connected to said reference bit line.

19. (original) The magnetic random access memory according to claim 1, wherein when the data stored in the selected cell is read out,

said second selector applies a read voltage to a selected word line and opens unselected word lines of the plurality of word lines other than said selected word line,

said first selector connects a selected bit line and a reference bit line to the read section,

said read section divides the voltage of the first power supply by said first tunneling magnetic resistance and said first resistance section of a selected cell to generate a sense voltage, divides the voltage of the first power supply by said reference tunneling magnetic resistance and said second resistance section of a selected reference cell to generate a reference voltage, and outputs a comparing result of said sense voltage with said reference voltage, and

said selected cell is selected from said plurality of memory cells by said selected word line and said selected bit line, and said selected reference cell is selected from said plurality of reference cells by said selected word line and said reference bit line.

20. (original) The magnetic random access memory according to claim 1, further comprising:

a plurality of second bit lines, each of which is paired with one of said plurality of bit lines and which extend in the second direction substantially perpendicular to the first direction;

a plurality of word lines extending in the second direction substantially perpendicular to the first direction;

a first selector configured to select said selected bit line from said plurality of bit lines;

a second selector configured to select said selected second bit line from said plurality of second bit lines; and

a third selector configured to select a selected word line from said plurality of word lines,

wherein each of said plurality of memory cells further comprises a first transistor and a second transistor,

said first transistor has a first gate connected to said word line, a first terminal serving as one of terminals other than the first gate connected to the bit line, and a second terminal serving as the other terminal,

said second transistor has a second gate connected to the word line, a fifth terminal serving as one of terminals other than the second gate connected to a second bit line, and a sixth terminal serving as the other terminal connected to the second terminal,

each of said plurality of memory cells is provided to one of positions where said plurality of bit lines, said

plurality of second bit lines, and said plurality of word lines are intersected,

said first tunneling magnetic resistance has a third terminal as one terminal connected to ground and a fourth terminal as the other terminal connected to said second terminal,

each of said plurality of reference cells further comprises:

a third transistor having a third gate connected to the word line, a seventh terminal serving as one of terminals other than the third gate connected to a bit line, and an eighth terminal serving as the other terminal;

a fourth transistor has a fourth gate connected to the word line, an eleventh terminal serving as one of terminals other than the fourth gate connected to the second bit line, and a twelfth terminal serving as the other terminal connected to the eighth terminal,

each of said plurality of reference cells is provided to one of positions where said reference bit line and said plurality of word lines are intersected, and

said reference tunneling magnetic resistance has a ninth terminal serving as one terminal connected to ground and a tenth terminal serving as the other terminal connected to the eighth terminal.

21. (original) The magnetic random access memory according to claim 20, wherein when the data stored in a selected cell is read out,

said first selector first selects a selected bit line and opens unselected bit lines of said plurality of bit lines other than said selected bit line,

said third selector supplies a voltage to said selected word line to turn on said first transistor and said second transistor of a selected cell, a voltage to unselected word lines other than said selected word line to turn off said first transistors and said second transistors of said unselected cells,

said read section divides the voltage of the first power supply by said first tunneling magnetic resistance and said first resistance section of said selected cell to generate said sense voltage, the voltage of the first power supply by said reference tunneling magnetic resistance and said second resistance section of said selected reference cell to generate said reference voltage, and outputs a comparing result of said sense voltage with said reference voltage,

said selected cell is selected from said plurality of memory cells by said selected work line and said selected bit line, the unselected cells are memory cells other than said selected cell, an the selected reference cell is selected from said plurality of reference cells by said selected word line and said reference bit line.

22. (previously presented) A magnetic random access memory comprising:

a selected cell having a first tunneling magnetic resistance;

a selected reference cell having a reference tunneling magnetic resistance; and

a read section,

wherein said read section comprises:

a first resistance section comprising at least one tunneling magnetic resistance, having a first resistance value and connected to said selected cell in a read operation;

a second resistance section comprising at least one tunneling magnetic resistance, having a second resistance value different from said first resistance value and connected to said selected reference cell in the read operation; and

a comparing section configured to compare a sense voltage at a cell node between said first resistance section and said selected cell with a reference voltage at a reference cell node between said second resistance section and said selected reference cell and to output the comparison result.

23. (previously presented) The magnetic random access memory according to claim 22, wherein said first resistance section comprises second and third tunneling magnetic resistances connected in series, and

said second resistance section comprises fourth and fifth tunneling magnetic resistances connected in series.

24. (previously presented) The magnetic random access memory according to claim 23, wherein said first to fifth tunneling magnetic resistances and said reference tunneling magnetic resistance have a same MR ratio dependency.

25. (previously presented) The magnetic random access memory according to claim 23, wherein said first to fifth tunneling magnetic resistances and said reference tunneling magnetic resistance have a same temperature dependency.

26. (previously presented) The magnetic random access memory according to claim 23, wherein said second and third tunneling magnetic resistances store data which is different from data stored in said reference tunneling magnetic resistance.

27. (previously presented) The magnetic random access memory according to claim 26, wherein one of said fourth and fifth tunneling magnetic resistances stores the data which is different from the data stored in said reference tunneling magnetic resistance, and the other stores the same data as said reference tunneling magnetic resistance.

28. (previously presented) The magnetic random access memory according to claim 22, wherein said first and second resistance sections are connected with a first power supply.

29. (previously presented) The magnetic random access memory according to claim 22, further comprising:

a first current mirror circuit connected to a second power supply to operatively connect said selected cell and said first resistance section; and

a second current mirror circuit connected to the second power supply to operatively connect said selected reference cell and said second resistance section; and

a constant voltage circuit provided between said first current mirror circuit and said selected cell and between said second current mirror circuit and said selected reference cell to supply a constant voltage to said selected cell and said selected reference cell.

30. (previously presented) The magnetic random access memory according to claim 29, wherein said constant voltage circuit includes a clamp circuit.

31. (previously presented) The magnetic random access memory according to claim 29, wherein said read section further comprises:

a first auxiliary section connected in parallel to said first current mirror circuit to change said sense voltage; and

a second auxiliary section connected in parallel to said second current mirror circuit to change said reference voltage.

32. (previously presented) The magnetic random access memory according to claim 22, further comprising first and second groups of resistance sections,

wherein each of said resistance sections of said first group is connected to a second switch operating in response to a second control signal,

said first resistance section is one of said first group of resistance sections associated with said second control signal,

wherein each of said resistance sections of said second group is connected to a third switch operating in response to a third control signal,

said second resistance section is one of said second group of resistance sections associated with said third control signal.

33. (previously presented) The magnetic random access memory according to claim 22, further comprising a memory cell array,

wherein said memory cell array comprises:

a plurality of read word lines extending in a first direction;

a plurality of bit lines extending in a second direction orthogonal to said first direction;

a plurality of memory cells respectively provided at positions where said plurality of read word lines and said plurality of bit lines are intersect;

a reference bit line; and

a plurality of reference memory cells respectively provided at positions where said plurality of read word lines and said reference bit line are intersect,

said selected cell is one of said plurality of memory cells associated with a specific one of said plurality of read word lines and a specific one of said plurality of bit lines in the read operation, and

said selected reference cell is one of said plurality of reference memory cells associated with said specific read word line.

34. (previously presented) The magnetic random access memory according to claim 22, further comprising a memory cell array, and a reference cell circuit,

wherein said memory cell array comprises:

a plurality of read word lines extending in a first direction;

a plurality of bit lines extending in a second direction orthogonal to said first direction; and

a plurality of memory cells respectively provided at positions where said plurality of read word lines and said plurality of bit lines are intersect,

said reference cell circuit comprises:

a reference bit line; and

a plurality of reference memory cells which are provided in parallel and each of which is connected to a first switch to activate said reference memory cell in response to a first control signal,

said selected cell is one of said plurality of memory cells associated with a specific one of said plurality of read word lines and a specific one of said plurality of bit lines in the read operation, and

said selected reference cell is one of said plurality of reference memory cells associated with said first control switch.

35. (previously presented) The magnetic random access memory according to claim 33, wherein said memory cell array further comprises:

a plurality of write word lines respectively provided for said plurality of read word lines to extend in said first direction.

36. (previously presented) The magnetic random access memory according to claim 33, wherein said memory cell array further comprises:

a plurality of second bit lines respectively provided for said plurality of bit lines to extend in said second direction.

37. (previously presented) The magnetic random access memory according to claim 22, wherein said first tunneling magnetic resistance can take a first state and a second state, and

said reference voltage Vref is obtained from the following equation (1):

$$Vref = Vs(1)+k\cdot(Vs(2)+Vs(1)) \qquad (1)$$

where said sense voltage in the first state is Vs(1), and said sense voltage in the second state is Vs(2) and a variable k is equal to or less than 0.49.